FIELD EFFECT TRANSISTOR

TECHNICAL FIELD

The present invention relates to a field effect transistor, in particular to a lateral field-effect transistor.

BACKGROUND ART

As to a lateral field-effect transistor, if an enlarged gate width is used to increase current capacity, a comb-shaped structure is often employed for source wiring and for drain wiring so that a plurality of transistor cells can be disposed to be connected in parallel. In such a case, as for gate wiring, a meander shape or a comb shape is employed.

A conventionally proposed field effect transistor has a top surface pattern formed in such a shape that digitiform portions of comb-shaped source and drain electrodes are disposed in opposed positions to interdigitate with each other, and a meander-shaped gate electrode is located between the source electrode and the drain electrode. Another conventionally proposed field effect transistor has digitiform portions of comb-shaped source and drain electrodes formed in an opposing manner to interdigitate with each other, digitiform portions of a comb-shaped gate electrode formed between the source electrode and the drain electrode, and common sections to serve as bases of the digitiform portions of the gate electrode and formed external to the transistor (for example, see Japanese Patent Laying-Open No. 2006-066887 (Patent Literature 1)).

A still another conventionally proposed transistor has a plurality of unit cells each having a source contact and a drain contact which are interdigitated, a gate contact situated between the source contact and the drain contact, and an overlayer electrically coupling the source contact to a p+ region via a p+ contact which is disposed in a contact via hole (for example, see International Publication No. WO 2006/065324 (Patent Literature 2)).

CITATION LIST

Patent Literature

PTL 1: Japanese Patent Laying-Open No. 2006-066887
PTL 2: International Publication No. WO 2006/065324

SUMMARY OF INVENTION

Technical Problem

Generally, it is understood that on the meander-shaped gate electrode disclosed in the document above, there is a gate wiring which is in the same meander shape as that of the gate electrode and has one end connected to a gate pad. If the gate wiring is in a meander shape, the gate wiring has a high resistance, and charging/discharging of a gate circuit takes time. In addition, the gate wiring has a longer length, which causes a time lag in a gate voltage change between a section of the gate wiring near the gate pad and another section distant from the gate pad. For these reasons, switching of the transistor cannot be speeded up.

Further, generally, the gate wiring has a width on the order of not more than 1 μm. Thus, during a manufacturing process, a missing pattern may occur, where wiring is partially not formed due to a failure in photolithography. If the gate wiring is in a meander shape, when the gate wiring breaks at even one point, a gate voltage does not change in a section of the gate wiring more distant from the gate pad than the point, and the transistor does not operate in that section. For this reason, an operationally defective transistor product tends to be produced.

Now, the comb-shaped gate wiring disclosed in the above-indicated Japanese Patent Laying-Open No. 2006-066887 (Patent Literature 1) has the digitiform portions of the gate wiring which run below the base of the source wiring. Usually, the base of the source wiring takes a large width, and therefore, the gate wiring running therebelow has a longer length and a higher resistance. Further, the gate wiring and the base of the source wiring have a larger intersecting area between them, which results in a larger gate-to-source capacity. For these reasons, charging/discharging of a gate circuit takes time, and switching of the transistor cannot be speeded up. In addition, due to a missing pattern occurred during a manufacturing process, the digitiform portions of the gate wiring break, the transistor does not operate in a section beyond the broken point, and an operationally defective transistor product tends to be produced.

The present invention has been made in view of the problems above, and an object of the invention is to provide a lateral field-effect transistor capable of improving switching speed and reducing operationally defective products.

Solution to Problem

A field effect transistor according to the present invention includes a substrate, an active layer formed on the substrate and a source wiring, a drain wiring and a gate wiring formed above the active layer. The source wiring is formed in a comb shape having a source wiring base and a plurality of source wiring fingers protruding from the source wiring base. The drain wiring is formed in a comb shape having a drain wiring base and a plurality of drain wiring fingers protruding from the drain wiring base. The source wiring and the drain wiring are arranged to oppose each other such that the source wiring fingers and the drain wiring fingers interdigitate. The gate wiring has a gate wiring base, a plurality of gate wiring fingers protruding from the gate wiring base, and a connection connecting tips of adjacent gate wiring fingers. The gate wiring finger is arranged between the source wiring finger and the drain wiring finger, and the gate wiring base is arranged between the source wiring base and the drain wiring fingers and intersects with the source wiring fingers, with an insulating film interposed between the gate wiring base and the source wiring fingers.

Preferably, adjacent gate wiring fingers and the connection connecting the gate wiring fingers make up a first wiring. A section of the gate wiring base between two points where adjacent gate wiring fingers connected by the connection are connected to the gate wiring base, respectively, makes up a second wiring which is electrically parallel with the first wiring. The first wiring has an electrical resistance not less than the electrical resistance of the second wiring.

Preferably, the gate wiring finger has a vertical cross-sectional area not more than the vertical cross-sectional area of the gate wiring base.

Preferably, the active layer includes a first conductivity type buffer layer, a second conductivity type channel layer formed on the buffer layer and having a surface, a second conductivity type source region formed from the surface of the channel layer opposing at least part of the source wiring finger to an interior of the channel layer, a second conductivity type drain region formed from the surface of the channel layer opposing at least part of the drain wiring finger to the